Remarks

In this discussion set forth below, Applicant does not acquiesce to any rejection or averment in the instant Office Action unless Applicant expressly indicates otherwise.

The instant Office Action dated July 11, 2008, lists the following rejections: claims 1-2, 10-20 and 27-29 stand rejected under 35 U.S.C. § 102(b) over Buer *et al.* (U.S. Patent No. 6,114,880); claims 3-6, 8-9, 21-23 and 25-26 stand rejected under 35 U.S.C. § 103(a) over Buer in view of Chuang *et al.* (U.S. Patent Pub. 2003/0128606); and claims 7 and 24 stand rejected under 35 U.S.C. § 103(a) over Buer and Chuang in view of Flautner *et al.* (U.S. Patent No. 7,278,080).

Applicant respectfully traverses the § 102(b) rejection of claims 1-2, 10-20 and 27-29 because the cited portions of the Buer reference do not correspond to numerous aspects of the claimed invention. The Examiner, in the instant Office Action, essentially repeats the rejections based upon Buer that were presented in the previous Office Action without responding to the substance of Applicant's arguments presented in the Response dated March 31, 2008 as required. *See, e.g.,* M.P.E.P. § 707.07(f) ("Where the applicant traverses any rejection, the examiner should, if he or she repeats the rejection, take note of the applicant's argument and answer the substance of it."). The Examiner continues to erroneously rely upon the same portions of the Buer reference while failing to reconcile the fact that these portions are not arranged in the manner required by the claimed invention. *See, e.g.,* M.P.E.P. § 2131 (In order to anticipate a claim, the elements of a prior art reference must be arranged as required by the claim.) Applicant submits that the Examiner has improperly continued to rely upon the same portions of Buer without responding to substance of Applicant's previous arguments. The following discussion particularly addresses the lack of correspondence between the cited portions of the Buer reference and the claimed invention.

The § 102(b) rejection of claims 1-2, 10-20 and 27-29 is improper because the rejection relies upon the erroneous assertion that Buer's known path generation circuit 14 provides a predetermined reference signal to Buer's critical path logic 20. As is shown by Buer in Figure 1 (reproduced below), Buer's known path generation circuit 14 is in parallel to Buer's critical path logic 20 and, as such, no signals are provided from known path generation circuit 14 to critical path logic 20.

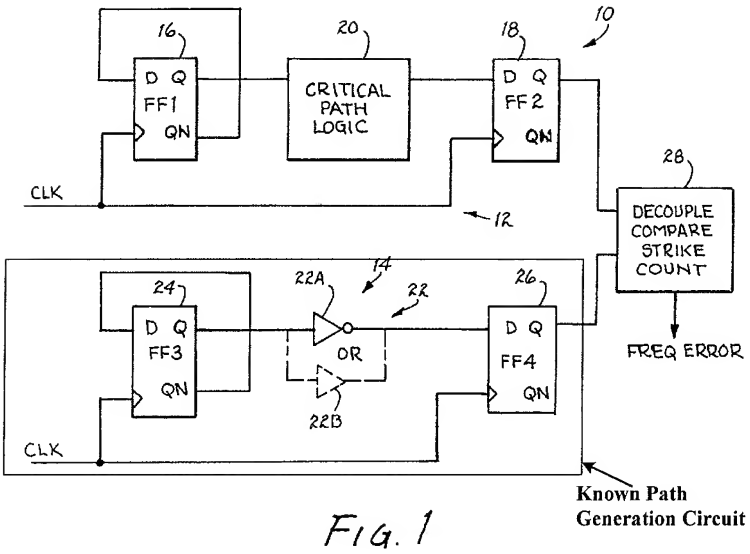

FIG. 1

According to M.P.E.P. § 2131, in order to anticipate a claim, the elements of a prior art reference must be arranged as required by the claim. In this instance, the claimed invention requires that the signal generator generate a reference signal which is provided by the signal generator to the duplicate logic path. As is shown in Buer's Figure 1, none of the signals that are generated by known path generation circuit 14 (*i.e.*, the Examiner's alleged signal generator) are provided to critical path logic 20 (*i.e.*, the Examiner's alleged duplicate logic path) because Buer's paths are arranged in parallel to each other. Thus, the cited portions of the Buer reference are not arranged as required by the claimed invention. Accordingly, the § 102(b) rejection of claims 1-2, 10-20 and 27-29 is improper and Applicant requests that it be withdrawn.

The § 102(b) rejection of claims 1-2, 10-20 and 27-29 is improper because the cited portions of Buer do not correspond to aspects of the claimed invention directed to the monitoring circuit providing a timing closure signal indicative of the status of the timing closure in the logic path being monitored responsive to comparing receipt of the output signal of the duplicate logic path to receipt of the clock signal. The Examiner asserts that Buer's comparator circuit 28 corresponds to the claimed monitoring circuit; however, the cited portions of Buer teach that comparator circuit 28 compares the output of known path generation circuit 14 to the output of critical path generation circuit 12 to generate a frequency error signal. *See, e.g.,* Figure 1 and Col. 4:9-30. Buer's comparator circuit 28 does not compare the receipt of the output signal of critical path logic 20 (*i.e.*, the Examiner's alleged duplicate logic path) to the receipt of clock signal CLK or to the

receipt of any other clock signal. Applicant notes that the Examiner merely cites to Buer's comparator circuit 28 and repeats selected claim language without providing any explanation regarding the apparent lack of correspondence between Buer's comparator circuit 28 and the claimed invention. As discussed above, Applicant submits that Buer's comparator circuit 28 does not compare the receipt of the output of the duplicate logic path to the receipt of the clock signal in order to produce the timing closure signal as in the claimed invention. Accordingly, the § 102(b) rejection of claims 1-2, 10-20 and 27-29 is improper and Applicant requests that it be withdrawn.

Applicant further traverses the § 102(b) rejection of claims 11-12 and 29 because the cited portions of Buer do not correspond to aspects of the claimed invention directed to the duplicate logic path including one or more buffer stages. The Examiner continues to erroneously assert that Buer's buffers 22 correspond to the claimed buffers of the duplicate logic path (*see, e.g.,* Figure 1 and Col. 3:64 to Col. 4:9). The cited portions of Buer teach that buffers 22 are part of known path generation circuit 14 (*i.e.,* the Examiner's alleged signal generator), not part of critical path logic 20 (*i.e.,* the Examiner's alleged duplicate logic path). Thus, the cited portions of Buer are not arranged as required by the claimed invention. *See, e.g.,* M.P.E.P. § 2131 discussed above. Accordingly, the § 102(b) rejection of claims 11-12 and 29 is improper and Applicant requests that it be withdrawn.

Applicant further traverses the § 102(b) rejection of claims 14 and 16 because the cited portions of Buer do not correspond to aspects of the claimed invention directed to the timing violation signal being supplied to a second timing closure monitoring circuit (claim 14), and one or more further timing closure monitoring circuits (claim 16). The Examiner continues to erroneously assert that Buer's protection circuit 30 corresponds to the claimed second timing closure monitoring circuit. The cited portions of Buer do not teach that protection circuit 30 has a duplicate logic path of a logic path being monitored or that protection circuit 30 has a signal generator that generates a predetermined reference signal. The known path generation circuit 14 (*i.e.,* the Examiner's alleged signal generator) and the critical path logic 20 (*i.e.,* the Examiner's alleged duplicate logic path) are not taught by Buer as being part of protection circuit 30. Thus, once again, the cited portions of Buer are not arranged as required by the claimed invention. *See, e.g.,* M.P.E.P. § 2131 discussed

above. Accordingly, the § 102(b) rejection of claims 14 and 16 is improper and Applicant requests that it be withdrawn.

Applicant respectfully traverses the § 103(a) rejection of claims 3-9 and 21-26 because the cited portions of the Buer reference do not correspond to the claimed invention as discussed above in relation to the § 102(b) rejection of claims 1 and 19. Applicant submits that neither the addition of the Chuang reference nor the addition of the Flautner reference overcome the above discussed deficiencies of the § 102(b) rejection of claims 1 and 19. In at least this regard, the § 103(a) rejections of claims 3-9 and 21-26 are improper because these claims depend from either claim 1 or claim 19. Accordingly, Applicant requests that the § 103(a) rejections of claims 3-9 and 21-26 be withdrawn.

Applicant further traverses the § 103(a) rejection of claims 3-6, 8-9, 21-23, 25 and 26 because the Examiner's fails to provided an adequate reason to combine the Buer and Chuang references. This approach is contrary to the requirements of § 103 and relevant law. *See, e.g., KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1741 (U.S. 2007) ("A patent composed of several elements is not proved obvious merely by demonstrating that each element was, independently, known in the prior art."). The Examiner asserts that the skilled artisan would be motivated to modify Buer, in some manner which the Examiner does not disclose, in order "to provide an unchanged select signal pulse width". *See, e.g.,* page 7 of the instant Office Action. As the cited portions of Buer do not mention any selection signal having a pulse width, the Examiner's unexplained conclusion does not provide support for how or why Chuang's unrelated teachings are combinable or otherwise (*see, e.g.,* paragraph 0046) applicable to the cited teachings of Buer. Applicant submits that the Examiner's alleged reason to combine is based upon unsupported conjecture in direct violation of the MPEP and the requirements of § 103.

The Examiner further asserts that the skilled artisan would be motivated to modify Buer in order "to improve overall performance, and enhance circuit robustness". *See, e.g.,* page 9 of the instant Office Action. Applicant submits that basing a § 103 rejection on conclusory statements regarding generalized advantages is contrary to the requirements of § 103 and relevant law. According to M.P.E.P. § 2142, however, "rejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to

support the legal conclusion of obviousness." In this instance the Examiner fails to provide any evidence that the proposed modifications of Buer would result in any of these alleged benefits. As such, the Examiner's proposed combinations are improperly based upon conclusory statements.

Moreover, the Examiner fails to provide any explanation regarding how the seeming unrelated teachings of the Buer and Chuang references are to be combined. In order to comply with 35 U.S.C. § 132, sufficient detail must be provided by the Examiner regarding the alleged correspondence between the claimed invention and the cited reference to enable Applicant to adequately respond to the rejections. *See, also,* 37 CFR 1.104 ("The pertinence of each reference, if not apparent, must be clearly explained and each rejected claim specified.") and M.P.E.P. § 706.02(j), ("It is important for an examiner to properly communicate the basis for a rejection so that the issues can be identified early and the applicant can be given fair opportunity to reply.") In this instance Applicant is unable to ascertain how the Examiner is proposing to combine the Buer and Chuang references. Applicant submits that the cited portions of Buer and Chuang do not provided clarification regarding how these seemingly unrelated teachings are to be combined. As such, Applicant requests clarification regarding which elements of Chuang are to be combined with Buer and how these elements are to be combined with Buer.

The § 103(a) rejection of claims 3-6, 8-9, 21-23, 25 and 26 is improper.

Applicant further traverses the § 103(a) rejection of claims 7 and 24 because the Examiner's fails to provided an adequate reason to combine the Buer and Flautner references. This approach is contrary to the requirements of § 103 and relevant law as discussed above. Examiner asserts that the skilled artisan would be motivated to modify Buer in order "to compensate additional time and power consumption in recovering the system when a failure occurs". *See, e.g.,* page 12 of the instant Office Action. The Examiner, however, fails to provide any evidence that the proposed modification would result in the alleged benefit and the Examiner's argument in this regard seems illogical in view of Buer's already provided solution. Applicant submits that Examiner's alleged reason to combine is once again based upon unsupported conjecture. Accordingly, the § 103(a) rejection of claims 7 and 24 is improper and Applicant request that it be withdrawn.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Aaron Waxler, of NXP Corporation at (408) 474-9063.

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